What is claimed is:

1. A modem, comprising:

a) a digital interface;

b) a receiver coupled to said digital interface; and

c) a transmitter coupled to said digital interface, said transmitter including an interleaver which receives incoming codewords having a plurality of symbols and a given length, wherein

said interleaver distributes said symbols according to

$$dL(i) = (D-1)*i, \quad i=0,1,2,\ldots,(N-1),$$

where dL(i) is the delay of the i'th symbol of a codeword, D is the interleaving depth, and N is said given length, and wherein

said interleaver includes N-1 registers for storing symbols of an incoming codeword in parallel, a plurality of said N-1 registers including a plurality of cells with each cell storing a symbol, and said interleaver further including a permutation register for storing indications of a static order in which symbols are either written into or read out from said plurality of registers in order to generate an interleaved outgoing codeword.

2. A modem according to claim 1, wherein:

said permutation register includes N-1 cells.

3. A modem according to claim 1, wherein:

each said outgoing codeword has N sequential symbols, and a first of said N sequential symbols is taken from a first symbol of said incoming codeword.

4. A modem according to claim 1, wherein:

each of said symbols is a byte.

5. A modem according to claim 1, wherein:

N is an odd number greater than five, and at least one of said plurality of N-1 registers has a single cell, at least one of said plurality of N-1 registers has two cells, and at least one of said plurality of N-1 registers has three cells.

6. A modem according to claim 5, wherein:

the length L_j of the j'th register of said N-1 registers is determined according to

$$L_j = \text{ceil}(j*D/N),\ j=1,2,\ldots,(N-1)$$

where ceil is a rounding-up to the next higher integer indication.

7. A modem according to claim 1, wherein:

said indications of said permutation register are set according to a code comprising

```
for n=0:1:(N*D - 1)
    f=n-N*floor(n/N);
    k=(D-1)*f + n;
    if k>N*(D-1) and k<N*D
        m=k-N*(D-1);
        P(m) = f;
    end
end
```

where P is said permutation register, and floor is a rounding down to the next whole number indication.

8. A modem according to claim 1, wherein:

said indications of said permutation register are set according to

$$f(n) = n_{ModN},$$

$$k(n) = (D-1)*f(n) + n,$$

$$m(n) = k(n) - N*(D-1),$$

where n=0,1,2,...,(N*D - 1), and Mod represents a modulus determination, and by setting indication f(n) into the m(n)'th cell of said permutation register when N*D>k(n)>N*(D-1).

9. A modem according to claim 1, wherein:

said plurality of said N-1 registers uses a total number of interleaver memory cells $m_I = (N-1)*[((D-1)/2) + 1)]$.

10. A modem according to claim 1, wherein:

said plurality of N-1 registers are implemented in one or more of FIFOs, shift-registers, circular buffers, and RAM.

11. A modem according to claim 1, further comprising:

a deinterleaver which receives interleaved codewords having said plurality of symbols and said given length, wherein said deinterleaver includes N registers for storing symbols of said interleaved codewords in parallel, a plurality of said N registers including a plurality of cells with each cell storing a symbol, and said interleaver further utilizing said indications of said permutation register in order to regenerate a deinterleaved codeword.

12. A modem according to claim 11, wherein:

the length LD_j of the j'th register of said N registers is determined according to $LD_j = D - \text{floor}(j*D/N), \quad j=0,1,2,\ldots,(N-1)$ where floor is a rounding down to the next whole number indication.

13. A modem according to claim 11, wherein:

each said regenerated deinterleaved codeword has N sequential symbols, and a first of said N sequential symbols is taken from a first delayed symbol of said interleaved codeword.

14. A modem according to claim 11, wherein:

each of said symbols is a byte.

15. A modem according to claim 11, wherein:

N is an odd number greater than five, and at least one of said plurality of N registers has a single cell, at least one of said plurality of N registers has two cells, and at least one of said plurality of N registers has three cells.

16. A modem according to claim 11, wherein:

said indications of said permutation register are set according to

$$f(n) = n_{ModN},$$

$$k(n) = (D-1)*f(n) + n,$$

$$m(n) = k(n) - N*(D-1),$$

where n=0,1,2,...,(N*D - 1), and Mod represents a modulus determination, and by setting indication f(n) into the m(n)'th cell of said permutation register when N*D>k(n)>N*(D-1).

17. A modem according to claim 11, wherein:

said indications of said permutation register are set according to a code comprising

```
for n=0:1:(N*D - 1)
    f=n-N*floor(n/N);
    k=(D-1)*f + n;
    if k>N*(D-1) and k<N*D
        m=k-N*(D-1);
        P(m) = f;
        P(0) = 0
    end
end
```

where P is said permutation register, and floor is a rounding down to the next whole number indication.

18. A modem according to claim 11, wherein:

said plurality of said N registers uses a total number of deinterleaver memory cells $m_D = (N-1)*[((D-1)/2) + 1)] + D$.

19. A modem according to claim 11, wherein:

said plurality of N registers are implemented in one or more of FIFOs, shift-registers, circular buffers, and RAM.

20. A modem, comprising:

a) a digital interface;

b) a transmitter coupled to said digital interface; and

c) a receiver coupled to said digital interface, said receiver including a deinterleaver which receives incoming interleaved codewords having a plurality of symbols and a given length, wherein said symbols were interleaved according to

$$dL(i) = (D-1)*i, \quad i=0,1,2,\ldots,(N-1),$$

where dL(i) is the delay of the i'th symbol of a codeword, D is the interleaving depth, and N is said given length, and wherein

said deinterleaver includes N registers for storing symbols of an incoming codeword in parallel, a plurality of said N registers including a plurality of cells with each cell storing a symbol, and said deinterleaver further including a permutation register for storing indications of a static order in which symbols are either written into or read from said plurality of registers in order to generate a deinterleaved codeword.

21. A modem according to claim 20, wherein:

said permutation register includes N cells.

22. A modem according to claim 20, wherein:

the length LD_j of the j'th register of said N registers is determined according to $LD_j = D - floor(j*D/N), \quad j=0,1,2,\ldots,(N-1)$ where floor is a rounding down to the next whole number indication.

23. A modem according to claim 20, wherein:

each said regenerated deinterleaved codeword has N sequential symbols, and a first of said N sequential symbols is taken from a first delayed symbol of said interleaved codeword.

24. A modem according to claim 20, wherein:

N is an odd number greater than five, and at least one of said plurality of N registers has a single cell, at least one of said plurality of N registers has two cells, and at least one of said plurality of N registers has three cells.

25. A modem according to claim 20, wherein:

said plurality of said N registers uses a total number of deinterleaver memory cells $m_D = (N-1)*[((D-1)/2) + 1)] + D$.

26. A modem according to claim 20, wherein:

said plurality of N registers are implemented in one or more of FIFOs, shift-registers, circular buffers, and RAM.

27. A method of interleaving codewords having a plurality of symbols and a given length N which are stored in a memory, said method comprising:

a) storing indications of a static order in which the symbols are to be written into or read from the memory in order to generate an outgoing interleaved codeword;

b) writing the codewords into the means with symbols of a given codeword located in parallel in the memory; and

c) reading the symbols out of the memory such that said symbols are distributed according to

$$dL(i) = (D-1)*i, \quad i=0,1,2,\ldots,(N-1),$$

where dL(i) is the delay of the i'th symbol of an outgoing codeword, and D is the interleaving depth,

wherein one of said writing and said reading is done in said static order.

28. A method according to claim 27, wherein:

N is an odd number greater than five,

said memory includes N-1 registers, and

at least one of said N-1 registers has a single cell, at least one of said N-1 registers has two cells, and at least one of said N-1 registers has three cells.

29. A method according to claim 28, wherein the memory includes N-1 registers, said method further comprising:

determining the length L_j of the j'th register of said N-1 registers according to L_j = ceil(j*D/N), j=1,2,...,(N-1),

where ceil is a rounding-up to the next higher integer indication.

30. A method according to claim 27, further comprising:

determining said indications of said static order according to a code comprising

```
for n=0:1:(N*D - 1)
     f=n-N*floor(n/N);
     k=(D-1)*f + n;
     if k>N*(D-1) and k<N*D
          m=k-N*(D-1);
          P(m) = f;
     end
end
```

where P is a permutation register for storing said indications of a static order, and floor is a rounding down to the next whole number indication.

31. A method according to claim 27, further comprising:

determining said indications of said static order according to

$f(n) = n_{ModN}$,

$k(n) = (D-1)*f(n) + n$,

$m(n) = k(n) - N*(D-1)$

where $n=0,1,2,\ldots,(N*D - 1)$, and Mod represents a modulus determination, and

setting indication $f(n)$ into the $m(n)$'th cell of a permutation register for storing said indications of a static order when $N*D>k(n)>N*(D-1)$.

32. A method of deinterleaving interleaved codewords having a plurality of symbols and a given length N, said interleaved codewords having been distributed in the interleaved codewords according to

$$dL(i) = (D-1)*i, \qquad i=0,1,2,\ldots,(N-1),$$

where dL(i) is the delay of the i'th symbol of an outgoing codeword, and D is the interleaving depth, said method comprising:

a) storing indications of a static order in which the symbols of the interleaved codewords are to be written into or read from memory in order to generate an outgoing deinterleaved codeword;

b) writing the interleaved codewords into the memory with symbols of a given codeword located in parallel in the memory; and

c) reading the symbols out of the memory to generate deinterleaved codewords,

wherein one of said writing and said reading is done in said static order.

33. A method according to claim 32, wherein the memory has N registers, said method further comprising:

determining the length LD_j of the j'th register of said N registers is determined according to $LD_j = D - floor(j*D/N)$, $j=0,1,2,\ldots,(N-1)$, where floor is a rounding down to the next whole number indication.

34. A method according to claim 32, wherein:

the memory has N registers, and N is an odd number greater than five, and at least one of said N registers has a single cell, at least one of said N registers has two cells, and at least one of said N registers has three cells.